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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	**Application No.** 09/903,208	**Applicant(s)** TOPHAM, NIGEL PETER
	Examiner Aimee J. Li	**Art Unit** 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-15 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32* is/are allowed.

6)☒ Claim(s) *1,3,5-15 and 30* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3, 5-15, and 30-32 have been considered. Claims 1, 3, 10, 14, 15 and 30 have been amended as per Applicant's request. New claims 31-32 have been added as per Applicant's request. Claims 16-29 have been cancelled as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 24 June 2005; Amendment as received on 24 June 2005; and Extension of Time for One month as received on 24 June 2005.

Claim Objections

3. Claims 1, 3, 14, and 15 are objected to because of the following informalities:

   a. Referring to claim 1, please make the following type of corrections. The corrections are underlined and bolded for insertions and double-bracketed or strikethrough for deletions.

      1) A processor adapted to receive instructions in one of first and second external instruction formats**,** F1 and F2**,** each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, and each **of** said external format**s,** Fl and F2, having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each **of** said opcode bit**s** in one of **said** external formats**,** F1 and F2**,** that has an individually corresponding opcode bit in the other one of external formats F1 and F2**,** being a common F1-F2 opcode bit in the format concerned so

that each **of said** external formats, F1 and F2, has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$, the processor comprising:

a) At least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

b) At least one instruction translation unit which employs the opcode bits to translate each instruction received in at least one of said external formats F1 and F2 into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

c) Wherein:

   i) Each **of** said first operations is specifiable in both said first and second external formats F1 and F2, and each **of** said second operations is specifiable in said second external format F2;

   ii) All **of** said first operations and all **of** said second operations have distinct opcodes in said second external format F2; and

   iii) For every one of the first operations which the processor is capable of executing, all the mutually-corresponding

common F1-F2 opcode bits in the two external formats F1 and F2 are identical to one another.

b. Claims 14, 15, 30, and 32 have similar grammatical and typographical errors, even though the limitations might not be the exact same, the language is similar and the grammatical and typographical errors are similar. So please correct those accordingly.

c. Referring to claim 3, please make the following type of corrections. The corrections are underlined and bolded for insertions and double-bracketed or strikethrough for deletions.

3) A processor as claimed in claim 1, also adapted to receive instructions in a third external instruction format F3, said third external format F3 having one or more preselected opcode bits in which an opcode, specifying the operation to be executed, appears, wherein:

iv) Each **<u>of</u>** said opcode bit**<u>s</u>** in one of said external formats F2 and F3 that has an individually corresponding opcode bit in the other one of the formats F2 and F3 is a common F2-F3 opcode bit in the format concerned so that each of said external formats F2 and F3 has, among its said one or more opcode bits, the same number C' of common F2-F3 opcode bits in total, where C' $\geq$ 1,

v) **<u>E</u>**ach **<u>of</u>** said execution unit receives instructions in at least one of first and second internal instruction formats**<u>,</u>** G1 and G2**<u>,</u>** and executes the operations specified thereby;

vi) Each **of** said second operations is specifiable in both said second and third external formats F2 and F3;

vii) Said at least one instruction translation unit translates an instruction specifying **one of** said first operations in either said first or second external formats F1 or F2 into said first internal format G1, and translates an instruction specifying **one of** said second operations in either said second or third external formats F2 or F3 into said second internal format G2; and

viii) For every one of the second operations which the processor is capable of executing, all the mutually-corresponding common F2-F3 opcode bits in the two external formats F2 and F3 are identical to one another.

4. Appropriate correction is required.

Allowable Subject Matter

5. Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claim 32 is allowed.

7. The following is an examiner's statement of reasons for allowance: As is indicated in the arguments there was nothing located in the prior art searched that the common opcode bits not only contained the same values but were also found in the exact same positions.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claim 10 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A signal cannot embody multiple instructions and is not considered a process, machine, manufacture, or composition of matter.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 14, 15, and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. In regards to claim 14, it is unclear how machine-readable medium described in the specification on page 29, lines 3-8 to include signals can store instructions. Signals cannot store instructions. Please amend the language to something similar to "machine-readable <u>storage</u> medium", which distinguishes the machine-readable medium described in the specification from the signals. Also, the preamble of the claim indicates that the invention being claimed is focused

on a machine-readable medium storing instructions, but there is also processor structure being claimed. It is unclear whether the claim is solely focused on the processor, the program stored on the machine-readable medium itself, or a processor using the instructions stored on the machine-readable medium.

10. In regards to claim 15, similar to claim 14, the preamble of the claim indicates a method of encoding processor instructions, but the body of the claim recites both processor structure limitations as well as what might be construed as method steps in the "wherein" clauses. It is unclear whether the claim is solely focused on a method of encoding processor instructions, the processor structure, or a processor executing the specific steps of the method.

11. In regards to claim 30, similar to claims 14, it is unclear how a signal can embody instructions, since instructions are usually a series of signals. Also, similar to claim 14 and 15, the preamble of the claim indicates a propagated signal embodying instructions, but the body of the claim recites processor structure and specific functions of the processor structure. Nowhere in the body of the claim is there any indication of propagated signals embodying instructions.

12. The Applicant is encouraged to contact the Examiner regarding the rejections above should there be any questions and/or clarification needed in regards to the problems with the claim language.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-4, 9-15, and 31-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Kissell, *MIPS16: High-Density MIPS for the Embedded Market.*

15. Regarding claims 1, 14 and 15, taking claim 1 as exemplary, Kissell has taught a processor adapted to receive instructions in one of:

a. First and second external instruction formats, F1 and F2 (see MIPS16 and MIPS, respectively, see p.4 lines 24-32), each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, (see p.5 lines 10-13), and each of said external formats, Fl and F2, having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each of said opcode bits in one of said external formats, F1 and F2, that has an individually corresponding opcode bit in the other one of external formats F1 and F2, being a common F1-F2 opcode bit in the format concerned so that each of said external formats, F1 and F2, has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$ (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)).

b. The processor comprising:

i. At least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby (see p. 4 lines 29-35 and Fig. 3); and

ii. At least one instruction translation unit which employs the opcode bits to translate each instruction received in at least one of said external formats F1 and F2 into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction (see Fig.3 and p.4 lines 29-35). Here, the internal pipeline executes instructions in the standard MIPS architecture, with MIPS16 instructions being translated (decompressed) into MIPS instructions, and 32-bit MIPS instructions are translated using a "null translation" into MIPS instructions for execution in the pipeline.

c. Wherein

i. Each of said first operations is specifiable in both said external formats F1 and F2 (see p.4 lines 30-32), and each of second operation is specifiable in said second external format F2 (see Fig.4 and p.5 lines 10-13). Here, any MIPS16 operation is specifiable in both MIPS16 format and MIPS format. However, certain MIPS operations (i.e. those that use longer opcodes, a register that is un-specifiable in MIPS16 instruction format (due to one bit fewer in its source/target register fields), those that use longer immediate values, or those that require 64-bit data words) cannot be specified in the MIPS instruction format.

ii. All of said first operations and all second operations have distinct opcodes in said second external format F2 (see Fig.4 and p.5 lines 10-13). Here, because any MIPS16 operation can be specified in the MIPS instruction format, but not all MIPS operations can be specified in MIPS16, any first operation that is specifiable by MIPS16 and MIPS (and can be directly translated as in Fig.4) inherently has a different opcode than an instruction not specifiable in MIPS16, otherwise the two operations would be identical.

iii. For every one of the first operations which the processor is capable of executing, all the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 are identical to one another (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)).

16. Claims 14, 15, and 30 are nearly identical to claim 1. Claim 14 differs in that it is comprised a machine-readable medium storing instructions to be executed, but its limitations encompass the same scope as claim 1. Claim 15 differs in that it is comprised as a method for encoding processor instructions, but its limitations also encompass the same scope as claim 1.

Claim 30 differs in that it is comprised as a propagated signal embodying instructions executed by a processor, but its limitations also encompass the same scope as claim 1. Therefore, claims 14 and 15 are rejected for the same reasons as claim 1.

17. Regarding claim 3, Kissell has taught a processor as claimed in claim 1, also adapted to receive instructions in:

a. A third external instruction format F3, (MIPS-III) (see p.4 lines 24-32 and p.5 lines 10-13),

b. Said third external format F3 having one or more preselected opcode bits in which an opcode, specifying the operation to be executed, appears (see "major opcode" of MIPS-III instructions on p.5 lines 10-13),

c. Wherein:

   i. Each of said opcode bits in one of said external formats F2 and F3 that has an individually corresponding opcode bit in the other one of the formats F2 and F3 is a common F2-F3 opcode bit in the format concerned so that each of said external formats F2 and F3 has, among its said one or more opcode bits, the same number C' of common F2-F3 opcode bits in total, where $C' \geq 1$ (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the

opcodes and as authorized by the MPEP § 2131.01(II)). Because MIPS-III instructions are directly translatable and 100% fully compatible with MIPS-I instructions (see Col.4 lines 24-32 and Col.5 lines 10-13), the opcode bits that MIPS-I/II instructions have in common with MIPS-III instructions are inherently identical as well.

ii. Each of said execution unit receives instructions in at least one of first and second internal instruction formats G1 and G2 and executes the operations specified thereby (see Fig.3 and p.4 lines 29-35). Here, the first internal format is considered to be what MIPS16 instructions are translated in, namely MIPS instructions using the MIPS16 Decompression Block (see Fig.3), and the second internal format is considered to be what MIPS-III instructions are translated into, also MIPS instructions, but using a "null translation".

iii. Each of said second operations is specifiable in both said second and third external formats F2 and F3 (see p.4 lines 24-32). Here, any MIPS16 operation is specifiable in MIPS16 instruction format, MIPS-I/II instruction format, and MIPS-III instruction format.

iv. Said at least one instruction translation unit translates an instruction specifying said first operation in either said first or second external format F1 or F2 into said first internal format G1, and translates instruction specifying said second operation in either said second or third external format F2 or F3 into said second internal format G2 (see Fig.3 and p.4

lines 29-35). Here, the first internal format is considered to be what MIPS16 instructions are translated in, namely MIPS instructions using the MIPS16 Decompression Block (see Fig.3), and the second internal format is considered to be what MIPS-III instructions are translated into, also MIPS instructions, but using a "null translation". Because a first operation (MIPS16) can be specified in MIPS16 or MIPS-I/II or MIPS-III formats, and a second operation (MIPS-I/II or MIPS-III) can be specified only in MIPS-I/II or MIPS-III formats, the first operation is translated into the format MIPS16 are translated into, and the second operation into the same format, although it is considered to be the format that MIPS-III instructions are translated into.

v. For every one of the second operations which the processors is capable of executing, all the mutually-corresponding common F2-F3 opcode bits in the two external formats F2 and F3 are identical to one another (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)). Because MIPS-III instructions are directly translatable and 100% fully compatible with MIPS-I instructions (see Col.4 lines 24-32

and Col.5 lines 10-13), the opcode bits that MIPS-I/II instructions have in common with MIPS-III instructions are inherently identical as well.

18. Regarding claim 9, Kissell has taught a processor as claimed in claim 1, wherein said first external format has an instruction width different from that of said second external format (see MIPS16 and MIPS, respectively, in Fig.4 and p.4 lines 24-29).

19. Regarding claim 10, Kissell has taught a processor as claimed in claim 1, wherein:

a. Said at least one translation unit (see MIPS16 Decompression Block in Fig.3) which performs a predetermined translation operation to translate each said external-format opcode into a corresponding internal-format opcode (see Fig.3 and p.4 lines 29-35). Here, the internal pipeline executes instructions in the standard MIPS architecture, with MIPS16 instructions being translated (decompressed) into MIPS instructions, and 32-bit MIPS instructions are translated using a "null translation" into MIPS instructions for execution in the pipeline.

20. Regarding claim 11, Kissell has taught a processor as claimed in claim 10, wherein said translation operation involves selecting and/or permuting bits amongst said preselected opcode bits in the external-format instruction (see Fig.4 and p.5 line 2 – p.6 line 2). Here, opcode bits of the MIPS16 instructions are selected and mapped into the internal MIPS instruction format during translation.

21. Regarding claim 12, Kissell has taught a processor as claimed in claim 10, wherein the translation operation is independent of the external-format opcode (see Fig.4 and p.5 lines 10-

13). Here, the translation is performed using a mapping, and thus is independent of the opcode value.

22. Regarding claim 13, Kissell has taught a processor as claimed in claim 12, wherein the translation unit identifies the internal format into which each external-format instruction is to be translated, and carries out said translation operation according to the identified internal format (see Figs.3-4, p.4 lines 30-33 and p.5 lines 10-13). Here, the MIPS16 Decompression Block identifies MIPS as the target internal format and translates MIPS16 instructions into MIPS instructions. Instructions that are already in uncompressed (MIPS) format can then be considered to use a "null translation" to be put into the internal format.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kissell, *MIPS16: High-Density MIPS for the Embedded Market,* as applied to claim 1 above, and further in view of Lin, U.S. Patent No. 6,633,969.

25. Regarding claim 5, Kissell has taught a processor as claimed in claim 1, but has not explicitly taught wherein the processor is a VLIW processor, wherein one external format is a scalar instruction format used for scalar instructions, and another external format is a VLIW instruction format used for VLIW instructions.

26. However, Lin has taught a VLIW processor with the ability to execute instructions in both long instruction word external formats (see Figs. 4B, 4D and Col.6 lines 12-48) and a scalar external formats (see Figs. 4A, 4C and Col.6 lines 12-48), allowing a 32-bit MIPS instruction to be produced every clock cycle so that processor throughput is increased (see Col.3 lines 1-16) while reducing the amount of storage space needed for the instructions (see Col.2 lines 1-39). One of ordinary skill in the art would have recognized that it is desirable to improve processor throughput, as well as to reduce instruction storage space required by a program. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Kissell to use VLIW instruction formats along with scalar instruction formats so that processor throughput can be increased and required storage space decreased.

27. Regarding claim 6, Kissell has taught a processor as claimed in claim 1, but has not explicitly taught wherein the processor is a VLIW processor, wherein the external formats are or comprise two different VLIW formats.

28. However, Lin has taught a VLIW processor with the ability to execute instructions in both long instruction word external formats (see Figs. 4B, 4D and Col.6 lines 12-48) and a scalar external formats (see Figs. 4A, 4C and Col.6 lines 12-48), allowing a 32-bit MIPS instruction to be produced every clock cycle so that processor throughput is increased (see Col.3 lines 1-16) while reducing the amount of storage space needed for the instructions (see Col.2 lines 1-39). One of ordinary skill in the art would have recognized that it is desirable to improve processor throughput, as well as to reduce instruction storage space required by a program. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Kissell to use

VLIW instruction formats along with scalar instruction formats so that processor throughput can be increased and required storage space decreased.

29. Regarding claim 7, Kissell in view of Lin has taught a processor as claimed in claim 6, wherein the two different VLIW formats are used in different respective instruction slots of a VLIW instruction parcel (see Fig. 4D). Here, the long instruction word parcel (instruction data block) contains both the 16-bit MIPS16 format (see Fig. 4B) as well as the 32-bit MIPS16 format (see Fig.4C) (see Col.6 lines 35-48)

30. Regarding claim 8, Kissell in view of Lin has taught a processor as claimed in claim 6, wherein at least one instruction slot of a VLIW instruction parcel uses the two different VLIW formats (see Fig. 4D). Here, the long instruction word parcel (instruction data block) contains both the 16-bit MIPS16 format (see Fig. 4B) as well as the 32-bit MIPS16 format (see Fig.4C) (see Col.6 lines 35-48).

Response to Arguments

31. Applicant's arguments filed 21 June 2001 have been fully considered but they are not persuasive. After careful review of the claim amendments and arguments clarifying the intention of the claim amendments, the amendments and arguments do not overcome the prior art cited.

32. Applicant argues in essence on pages 14-18

> ...The definition of the common opcode bits in the amended independent claims also specifies that "each external format F1 and F2 has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$".
>
> ...

> ...The opcode bits of the MIPS 16 instruction are all in different bit positions from the opcode bits in the 32-bit MIPS instruction. Thus, it appears that the opcode bits in the MIPS 16 format and the 32-bit MIPs format are not "common opcode bits" in the sense required by the amended independent claims.
>
> ...
>
> ...For example, it appears that the instruction translation unit in the MIPS processor may have to partially decode the instruction to translate it and/or may need to use some form of look-up table. In the present invention, on the other hand, because the common opcode bits are identical for every first operation, no such decoding or look-up table is necessary.

33. This has not been found persuasive. The arguments presented regarding the language seem to be directed towards limitations not explicitly cited in the claim language. The limitations present in the arguments above may be insinuated from the claim language as they stand. The most general and broadest reasonable interpretation of the claim language is that there are two instruction formats that has one or more opcode bits. The two instruction formats also has one or more opcode bits in common between the. The claim language is unclear as to whether these opcode bits, for every instruction, must be the exact same one or more locations between the two instructions formats. As is stated in the arguments on pages 15-16, there are certain instructions where the common opcode bits are incidentally the same and in the same location for one or more bits. This claim limitation is not present until dependent claim 31, which has been objected to. Even then, there is nothing the claim language to suggest that they are also purposefully the exact same between the two instruction formats, as insinuated by the

arguments. Also, the translation aspects stated on pages 16-17 are not in the claim language. There is nothing in the claim language to indicate whether the need to partially decode an instruction to translate it and/or use of a look-up table is necessary or not. In general, the limitations relied upon in the arguments are not clearly and specifically recited in the claim language. Should the limitations relied upon in the arguments be incorporated into the claim language, then the prior art would not be applicable.

34. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the above cited arguments) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

35. Applicant is encouraged to contact the Examiner regarding the claim language to clarify what Applicant's are arguing in the claim language and with regards to the typographical and grammatical errors.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Advanced RISC Machines Limited's (ARM®) "Atmel Corporation ARM7TDMI™ (Thumb®) Datasheet" from January 1999 and "Thumb®

Instruction Set Quick Reference Card" has taught an instruction format with common opcode bits, but not necessarily in the same positions.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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